

**REMARKS**

In the office action of March 6, 2006, to which this is a response, Examiner stated:

Applicants are required to cancel these nonelected claims (1-10) or take other appropriate action.

In response, Applicants point out that they already canceled "these claims (1-10)" in their previous response in which they elected claims 11-20. A review of that response will show not only that applicants indicated in their listing of the claims (on page 2) that claims 1-10 were canceled, but that they also specifically stated the cancellation in their REMARKS on page 5. Applicants continue to list claims 1-10 as canceled in the present response.

Applicants have amended the title of the application as suggested by Examiner.

Applicants have amended claim 11 as indicated in the Listing of the Claims.

Claims 11-20 only are presented. These claims stand rejected as obvious under 35 USC 103(a) over Fukumoto et al (US 2002/0105068) in view of Brandenburg et al (US 6,180,045). Applicants traverse this rejection.

Applicants claim a METHOD of developing an electronic module. In applicants' independent claim 1, the first step of this method is providing a developmental unit of the electronic module, the developmental unit comprising a motherboard, a multichip module, and a circuit unit connected to the multichip module. The circuit unit comprises structure including instrumentation circuitry on a flexible substrate that is not mounted directly to the motherboard. The instrumentation circuitry is needed only in the development process; and the second step of claim 1 produces a production unit of the electronic module by eliminating the circuit unit without altering the motherboard.

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Examiner's rejection is directed mainly to the first step of this two step method, with the references each describing structure allegedly the same as that recited by applicants in the developmental unit of their first step. But neither reference discloses anything about providing a first version of an electronic module including a circuit unit comprising instrumentation circuitry not directly mounted to a motherboard of the module for developmental purposes and easily removed, without modification of the motherboard.

Examiner's support for allegedly a suggestion of applicants' second step in Fukumoto et al is found in the following statement of the Examiner:

producing a production unit of the electronic module by eliminating or increasing the circuit to vary the stacked semiconductor device structure (Page 1, paragraph 2) without altering the motherboard.

But here is the actual language of Fukumoto et al, page 1 paragraph 2:

[0002] The present invention relates to a surface mount type stacked semiconductor device structure including a plurality of semiconductor devices each having a package and an outer lead, in which space for mounting the semiconductor devices on a system appliance can be reduced and capacity of the semiconductor devices can be increased.

This paragraph, along with the rest of the reference, teaches semiconductor structures that save motherboard space by vertical stacking, but does not teach eliminating circuitry from a previous, developmental version of the structure. There is no suggestion whatever that any element of the structure is or was needed only for developmental purposes or that any element of that structure is to be eliminated from a production version of the structure. This is likewise true for the other reference Brandenburg et al 6, 180,045.

Applicants recite in their second step:

...producing a production unit of the electronic module by eliminating the circuit unit without altering the motherboard.

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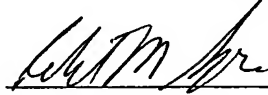
The recitation of the circuit unit refers back to the same element in the first step, where it is recited as a circuit element comprising, among other elements, instrumentation circuitry required only in the developmental unit. This underlined recitation, while previously implicit in the claim in view of the specification, has been added by amendment in this response to make explicit the difference between this claim and the cited references.

Applicants further point out that, although Examiner characterizes circuit elements in the Fukumoto et al reference as being “instrumentation circuitry” as recited by applicants, there is no evidence in either reference that any circuit elements therein are indeed such “instrumentation circuitry” or that any circuitry is used only in development and not in the production module. Even if instrumentation circuitry for developmental purposes is known in the art, this does not, by itself, inherently provide a teaching that there was a prior, developmental version of the structure in which instrumentation circuitry required for developmental purposes was present, connected to but not directly mounted on, a motherboard of the module but was then removed from the production version without modification of the tested and validated circuitry on the module motherboard. A reliance based on such a teaching to reject applicants’ method claims appears to be based only on hindsight in view of applicants’ own disclosure.

Neither of the cited Fukumoto et al or Brandenburg et al references teaches a two step process in which a developmental version of an electronic module is produced including a circuit element including instrumentation circuitry required only in the developmental module and connected to but not mounted directly on a motherboard of the module and a production version is then produced in which the circuit element is eliminated without altering the motherboard. Examiner’s rejection is without support in the cited prior art and should be withdrawn. Applicants thus believe that their claims are in condition for allowance.

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Respectfully submitted,

A handwritten signature in black ink, appearing to read 'R. M. Sigler', is written over a horizontal line.

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